REMARKS

Claims 1-12 and 16-30 are pending. The Examiner's reconsideration of the rejections is respectfully requested in view of the remarks.

Claims 1, 16, and 28 have been objected, wherein the Examiner suggested that the phrase "outputting a transformed hierarchical VLSI design" is not clearly described in the specification.

Applicants respectfully disagree; outputting a transformed hierarchical VLSI design is described at, among other places, page 6, lines 3-6, and page 45 lines 18-20. Further, an illustrative example is given at page 7, line 20 to page 8, lines 3, for example, "the isomorphism of the processed hierarchical graph is performed 309 and the processed hierarchical graph is stored in a corresponding database." Given the foregoing exemplary portions of the disclosure, Claims 1, 16, and 28 are believed to have clear support in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description as required under 37 C.F.R. 1.75. Reconsideration of the objection is respectfully requested.

Claim 28 has been objected to wherein the Examiner suggested that the phrase "a more operation, a split operation or a merge operation" is an incomplete claim structure as the object of the operations is not claimed.

Claim 28 claims, *inter alia*, "representing a structure of the hierarchical very large scale integrated design as a graph comprising design objects; specifying a transformation behavior applied to the design objects; processing the graph top-down beginning with a root cell of the graph to perform the transformation behavior on the hierarchical very large scale integrated design, wherein the transformation behavior resolves a boundary condition of the hierarchical very large scale integrated design by performing a move operation, a split operation or a merge operation to adjust the structure of the hierarchical very large scale integrated design."

It is clear from Claim 28 that a structure of the hierarchical very large scale integrated design is represented as a graph comprising design objects, and that the graph is processed by performing a move operation, a split operation or a merge operation. Thus, the move, split and merge operations are performed on the graph representing the hierarchical very large scale integrated design. The Examiner's reconsideration of the objection is respectfully requested.

Claims 1-12 and 16-30 have been rejected under 35 U.S.C. 102(b) as being anticipated by Russell et al. (U.S. Patent No. 5,519,628). The Examiner stated essentially that Russell teaches all the limitations of Claims 1-12 and 16-30.

Claims 1 and 16 claim, *inter alia*, "specifying a transformation behavior applied to the design objects; processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design; and outputting a transformed hierarchical very large scale integrated design." Claim 28 claims, *inter alia*, "specifying a transformation behavior applied to the design objects; processing the graph top-down beginning with a root cell of the graph to perform the transformation behavior on the hierarchical very large scale integrated design, wherein the transformation behavior resolves a boundary condition of the hierarchical very large scale integrated design by performing a move operation, a split operation or a merge operation to adjust the structure of the hierarchical very large scale integrated design; and outputting a transformed hierarchical very large scale integrated design."

Russell teaches methods for VLSI circuit design checking (see col. 6, liens 26-37). Russell does not teach, "processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design" as claimed in Claims 1 and 16 and essentially as claimed in Claim 28. Russell teaches a top-down search in building a list of shape instances (LISA) (see col. 22, lines 14-28). The building of the LISA is not analogous to performing a

transformation behavior on a hierarchical very large scale integrated device, essentially as claimed in Claims 1, 16, and 28. The top-down search for shape instances does not perform a transformation behavior; according to Russell, processing occurs in a bottom-up method. For example, see Figures 55 and 56 wherein after a search has been performed at 5502, a graph is modified, e.g., deleting a subgraph, by traversing an ancestor path 5628 (see col. 31 lines 39-41 and col. 32 lines 4-8). Traversing the ancestor path is a bottom-up processing beginning with leaf nodes. Russell does not teach, "processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design" as claimed in Claims 1 and 16 and essentially as claimed in Claim 28. Therefore, Russell fails to teach all the limitations of Claims 1, 16, and 28.

Claims 2-11 depend from claim 1. Claims 17-27 depend from claim 16. Claims 29 and 30 depend from Claim 28. The dependent claims are believed to be allowable for at least the reasons given for Claims 1, 16, and 28. Reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the present application, including claims 1-12 and 16-30, is believed to be in condition for allowance. The Examiner's early and favorable action is respectfully urged.

Respectfully submitted,

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